REMARKS

Claims 1-22 are pending. Applicants have canceled claims 1-6, amended claims 8 and 9, and added claims 23-28. No new matter has been added.

The Examiner has rejected all claims under 35 U.S.C. § 103(a) as follows:

Claim Nos.	*Combination of References*
1-5	Leung (6,415,353) and Amitai (4,797,850)
7-13	Leung, Amitai, and Miller (5,987,577)
6 and 14	Leung, Amitai, Miller, and Getzinger (4,972,314)
15 and 20	Leung, Amitai, and Miller
16-19 and 21-22	Leung, Amitai, Miller, and Getzinger

Applicants respectfully disagree.

In previous responses and briefs, applicants have consistently argued that Leung and Amitai, either alone or in combination, do not disclose analogous structure or functionality to that claimed by applicants. Specifically, applicants have continued to draw a distinction between not enabling access to a section of memory and not accessing a section of memory. In the former, access to the section of memory cannot be achieved even when that section of memory is being addressed. In the latter, access can be achieved, but is not done so because the memory location associated with a portion of the memory is not being addressed. Both Leung and Amitai operate in the latter fashion, that is, by limiting the access to memory locations within the device based on the utilized addresses. In Leung, data may be read from a memory address corresponding to one of the 64 DRAM banks. In Amitai, data may be read from an individual bit of a multiple-byte

data word in memory based on a memory address. In contrast, applicants operate in the former fashion, not enabling access to selected memory locations. Applicants respectfully submit that there is no corresponding structure or functionality provided in Leung or Amitai that disables access to a portion of the memory. Leung and Amitai both fail to disclose disabling a section of the memory in a fashion that precludes data retrieval from the section and reduces power consumption.

The Examiner has further suggested that Miller discloses preserving power by "not enabling a section of a memory bank representing a subdivision of a word of memory, and disabling row enable lines to a section of a memory bank representing a subdivision of a word of memory." (Office Action, p. 8.) Miller discloses a DRAM architecture that has two row enable inputs. (Miller, col. 9, line 65 – col. 10, line 1.) The first enable input causes an address to be applied to the row precoder, while the second enable input causes the row to be enabled. (Id. at col. 10, lines 1-12.) The purpose of such an architecture is to increase the speed of the DRAM when used in high speed cache applications. (Id. at col. 10, lines 12-14.) Miller does not disclose disabling access to a section of memory representing a subdivision of a word in a fashion that precludes data retrieval from that section. When addressing ancillary benefits, Miller indicates that power is conserved in the event that a full array access does not occur. (Id. at col. 10, lines 39-42.) As noted above, not accessing memory to save power (as is disclosed in Miller) is different that applicants' method of not enabling access to a section of memory which thereby saves power.

Moreover, the technology disclosed in Leung, Amitai, or Miller would not suggest applicants' solution. Leung's stated purpose is to enable a memory containing DRAM cells to operate like a SRAM device. Amitai's stated purpose is to enable addressing at the byte level. Miller's stated purpose is to increase speed with respect to DRAM access in high speed cache applications. None of the references suggest techniques for reducing power or allowing multiport operation as are claimed by applicants. Applicants therefore respectfully submit that one would not look to Leung, Amitai, or Miller for possible solutions to the problem addressed by applicants' technology. Since the Examiner has failed to

present a *prima facie* case of obviousness, the pending claims should therefore be allowed.

Claim 8 has been amended to correct a grammatical error, and claim 9 has been amended to further define the claimed invention.

New claims 23-28 are added in this Response. Among other reasons, new independent claim 23 is allowable over Leung, Amitai, Miller and the other references because the references fail to disclose or suggest the recited limitation of a memory bank having a plurality of sections wherein enabling logic generates signals so that "a section is enabled when a subdivision of a word contained within the section is accessed, and a section is disabled to reduce power consumption when a subdivision of a word contained within the section is not being accessed." The dependent claims contain additional limitations that further distinguish applicants' invention over the cited art.

For the reasons set forth herein, applicants request that the outstanding rejections be withdrawn. By focusing on specific claims and claim limitations in the discussion above, applicants do not intend to imply an agreement with the Examiner's assertions regarding other claims and claim limitations.

If the Examiner believes that a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206)359-3129. Otherwise, applicants respectfully request reconsideration of the application and its early allowance.

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Respectfully submitted,

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